Computer-Aided Design of Step Recovery Diode Frequency Multipliers

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Abstract—**Through the study of the step recovery diode (SRD) models, a method for improving the efficiency of CAD of SRD frequency multipliers is proposed. By reducing the nonlinearity of the SRD model to an appropriate extent, the simulation and optimization of SRD frequency multipliers can be carried out more easily and faster. Systematic design and optimization of an SRD frequency multiplier is described. Simulation results of this SRD frequency multiplier are compared with experimental results.**

I. Introduction

ONE OF THE most outstanding characteristics of the step recovery diode (SRD) is the high conversion efficiency with high frequency multiplication order. It provides a method for generating power at high frequencies by using a low cost oscillator. SRD frequency multipliers are typically used in hybrid local oscillators, especially where low phase noise is required: in terrestrial communications, satellite communications, TVRO, mobile communications. Input frequencies could extend down to 10 MHz and output frequencies up to 94 GHz [1], [2].

Another typical application of the SRD is as a comb generator in microwave and millimeterwave samplers, which are used in frequency counters, sampling scopes, phase locked synthesizers, and network analyzers [3]–[5].

In the past, designs of SRD frequency multipliers were mainly based on the method of Hamilton and Hall [6]. In this approach, the SRD was modeled as an ideal conductor for the conducting state and a capacitor for the nonconducting state. By this assumption, the SRD frequency multiplier could be simplified to two separate circuits called the input circuit and the output circuit. The advantage of this approach is the simplicity of the analysis.

However, in real circuits the SRD does not act like a simple switch between the conducting state and the nonconducting state. The transition from the conducting state to the nonconducting state has a finite transition time [7]. Furthermore, the input and output circuits affect each other in a complicated way. Therefore, a circuit designed by this method must be adjusted experimentally. Good performance could still be achieved by cut and try. And if the circuit were built in waveguide, we would have more flexibility for adjusting it.

With the increasing demand of integrated circuits, more accurate designs are required to develop the circuits in a medium where adjustment is not possible. Of course, there are other reasons which influence the medium of the circuit; microstrip circuits have small size, low weight, high reliability, while waveguide has low loss and high power handling capability. In parallel, the development of computer technology and computer-aided design tools provides us with the possibility of the simulation and optimization of the circuits to achieve an accurate design and optimum performance.

Moreover, the idealized model used in the method of Hamilton and Hall cannot be used directly in commercial circuit simulators, since the circuit-solving algorithms used by simulators are based on algorithms like the Newton-Raphson algorithm. The constitutive relationships of the device must be differentiable with respect to voltage and current, and these derivatives must also be continuous with respect to voltage and current.

To realize the CAD of SRD circuits, we developed a new SRD model which is more accurate by considering the voltage ramp during the transition process, and which can be directly used in commercial circuit simulators [8].

However, SRD frequency multipliers cannot be analyzed as readily as varactor or resistive diode multipliers [9]. Harmonic-balance analysis of the SRD frequency multiplier can be troublesome because of the strong nonlinearity of the diode, the large number of harmonics involved, and the possible instability make convergence precarious. In addition to choosing an advanced simulator for good convergence, other efforts should be made to find the correct solution efficiently for this type of circuit.

In order to improve the efficiency of CAD of SRD frequency multipliers, we have investigated the modeling of the diode and characteristics of SRD frequency multipliers. The results show that reducing the nonlinearity of the model of the diode to some extent while optimizing the circuit does not change the characteristics of the circuit radically. On the other hand, the efficiency of the CAD of this kind of circuit is greatly improved and the analysis itself is more easily and faster accomplished.

In this paper, we shall first discuss the modeling of the SRD. Then, the method of reducing the nonlinearity of the model is proposed and the simulation results with different degrees of nonlinearity of the model are compared. A systematic design of an SRD frequency multiplier is given as an example. Finally, the simulation results of this SRD frequency multiplier are compared with experimental results.

II. Nonlinearity of SRD

The SRD, which is also called the snap-off diode or charge storage diode, was first recognized in the early 1950's. The diode was modeled in a way that it behaves as a two-state

Manuscript received March 25, 1996.

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Publisher Item Identifier S 0018-9480(96)08529-8.

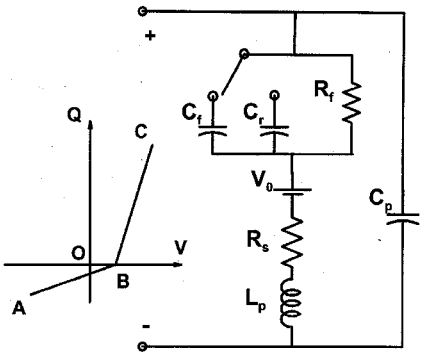

Fig. 1. Conventional model of SRD.

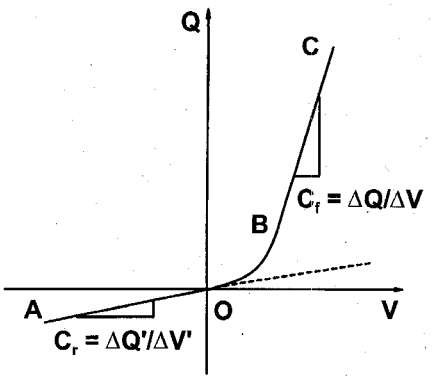

Fig. 2. Modified model of SRD.

capacitor of large capacitance (forward bias capacitance C_f) under forward charge storage state and small capacitance (reverse bias capacitance C_r) under reverse bias, with zero switching time between states, as shown in Fig. 1. Analyzes of resonant and nonresonant circuit performance using this model describe the first-order diode behavior very well [6], [7].

Nevertheless, the forward state capacitance, which is a diffusion capacitance determined by a large number of free carriers in a finite volume, can not physically be infinite. The transition time, in which an SRD switches between forward and reverse states, cannot be zero, either.

The transition process was studied and modeled by Moll and Hamilton [7]. Based on it, a new model was established by Zhang and Räisänen [8]. During the transition process, the voltage (V) across the diode and the stored charge (Q) in the intrinsic or lightly doped layer can be described approximately by

$$V = \frac{I_R}{\varepsilon v A}\left[\frac{W^2}{4} - W\sqrt{Q}\sqrt{\frac{2D}{I_R}}\right] \tag{1}$$

where v, A, and D are the average velocity of carriers in the space charge limit range, the working area of the diode and the ambipolar diffusion constant, respectively. I_R is the reverse current when the diode is reverse biased. W is the width of the field free intrinsic center region.

Examining (1) we can see that this transition process can be described by a parabolic function, which can be determined by the two state capacitance corresponding to the conducting state (C_f) and nonconducting state (C_r) of the diode, respectively.

Using the continuity conditions at the points where the transition starts and ends, we obtain the equation describing this transition process

$$Q = \begin{cases} C_r V & V \le 0 \\ \frac{C_f - C_r}{2\phi}\left(V + \frac{C_r \phi}{C_f - C_r}\right)^2 - \frac{C_r^2}{2(C_f - C_r)} \cdot \phi & 0 < V < \phi, \\ C_f V - \frac{C_f - C_r}{2} \cdot \phi & V \ge \phi \end{cases} \tag{2}$$

where ϕ is the contact potential at which the transition starts.

The characteristic of the diode, illustrated in Fig. 2, shows that the nonlinearity of the diode model is closely related to the forward bias capacitance C_f. While modeling the diode, we can extract this parameter through a DC measurement on the SRD. When the SRD is forward biased, the p-n junction acts like a dynamic or nonlinear resistor (R_f). The relationship of

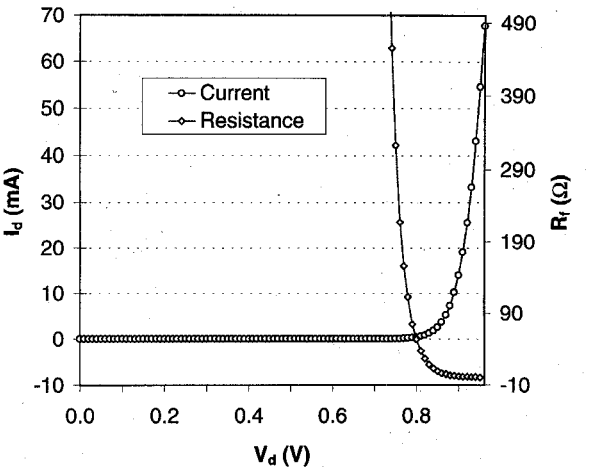

Fig. 3. *I-V* curve of SRD (HP-5082-0835).

C_f, R_f and the minority carrier lifetime τ can be related as given by Kotzebue [10],

$$\tau = R_f C_f \tag{3}$$

where τ is usually given by the manufacturer, and R_f can be obtained from the *I-V* characteristic of the SRD.

We have measured an SRD (HP-5082-0835) made by Hewlett-Packard, and its *I-V* curve is shown in Fig. 3. It can be seen that the forward bias resistance turns into a very small and nearly constant resistance right after the diode is forward biased. In this case, the value of the forward resistance is of the order of 0.1 ohm, which corresponds to a forward bias capacitance C_f of 100 nF. The minority carrier lifetime τ of 10 ns is given by the manufacturer.

However, the depletion capacitance of this diode, which is used as the reversed bias capacitance C_r in our model, is given as about 0.3 pF. Comparing with the calculated C_f above shows the very strong nonlinearity of the diode model. Directly using this model in circuit simulators would definitely cost a lot computational resources and most probably cause convergence problems.

In the simulation of circuits, good initial conditions are sometimes critical for convergence. Besides that, they often help the simulator use less computational resources (time and memory) to find the correct solution. Normally, there is a way to set initial conditions in the simulator. Using a simplified

or less ill-behaving circuit is one way to find good initial conditions.

Another process for obtaining convergence when simulating circuits is to start with values of certain components that work and then to move toward the desired values. For instance, in an amplifier circuit there may be a resistor that can be used to lower the amplifier's gain. The simulator may be able to find a solution to the circuit under a low-gain condition. Then, if the component's value is swept toward the desired value, the simulator may be able to find a final solution.

From the characteristic of SRD shown in Fig. 2 we know that the smaller is the forward bias capacitance, the less nonlinear is the diode model. Thus, we can at first reduce the nonlinearity of the diode model by changing the forward bias capacitance to a smaller value. The reduction of the nonlinearity of the model may very possibly help the simulator to find a solution, which can be used to obtain the desired final solution efficiently.

In order to find a solution to our problem, we have investigated the effect of changing the forward bias capacitance to a smaller value while modeling the diode. At first, we investigated the effect of the reduction on the circuit characteristics. Taking the SRD HP-5082-0835 as an example, we know that the forward bias capacitance (C_f) is about 100 nF, while the reverse bias capacitance (C_r) is about 0.3 pF. Using the equivalent circuit in Fig. 1 to calculate the input impedance in the forward charge storage state, we can see that, when the fundamental frequency is high enough, e.g., 1 GHz or higher, and C_f larger than 0.1 nF, C_f actually does not contribute much to the input impedance with typical parasitic parameters $C_p = 0.2$ pF, $R_s = 1.3\ \Omega$, and $L_p = 1$ nH. And in the reverse bias state, the characteristic of the diode depends only on the reverse bias capacitance C_r. Therefore, if we change C_f to an appropriate lower value according to the fundamental frequency, the characteristic of the circuit will not be radically changed. However, as we shall see in the following simulations, the simulation of the circuit is much faster and easier.

It should be noted that the calculation of the forward bias capacitance by using the *I-V* curve is approximate. The relationship described by (3) was obtained under the assumption of zero transition time. From the *I-V* characteristic of the diode shown in Fig. 3 we can see that the highly nonlinear capacitance characteristic is accompanied by a highly nonlinear shunt resistance which depends on the forward bias voltage and RF input power. Therefore, the degree of reduction depends on how much C_f is changed, and the operating conditions of the diode. More accurate method of extracting the parameter C_f should be studied in the future.

III. Design and Simulation of SRD Frequency Multiplier

Based on the SRD model proposed by Zhang and Räisänen [8], the simulation is directly done with the HP Microwave and RF Design System® (MDS), on a HP workstation (HP 85 180). A systematic design of the SRD frequency multiplier is given first.

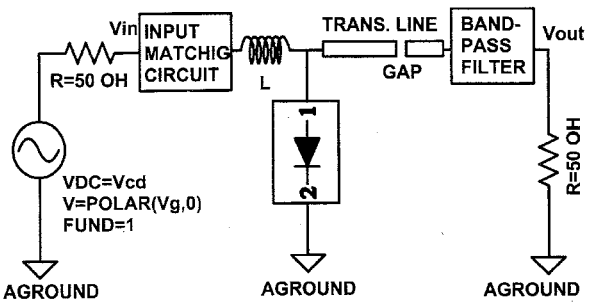

Fig. 4. Schematic ofthe SRD frequency multiplier circuit.

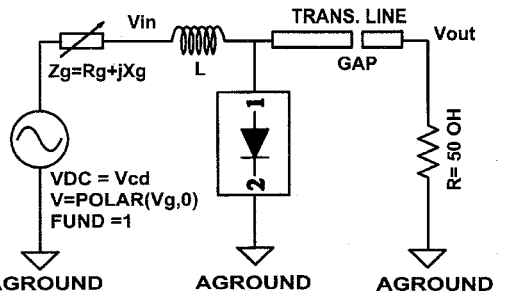

Fig. 5. Simulation circuitfor determining optimum source impedance.

The SRD frequency multiplier can be divided into two parts: the comb generator, which is rich in harmonics of fundamental frequency; and the bandpass filter, which is used to extract the desired harmonic from the output of the comb generator. The circuit is illustrated in Fig. 4, in which the bandpass filter and the output circuit of the comb generator, namely the transmission line and gap, form the output circuit of the frequency multiplier.

Normally, the output circuit of the comb generator is simply a piece of 50 Ω transmission line. Here, a gap is added in the transmission line, which can be used to block the DC and partially reflect the RF output. It also provides us with more design freedom for optimization of the circuit.

When the output circuit of the comb generator is chosen, a corresponding input circuit can be designed. First, the driving inductor L in Fig. 4 can be estimated by using Hamilton and Hall's method [6]. The details of the calculation are omitted here, but are shown in [11]. Then, the input matching circuit can be designed by using MDS.

The circuit used for determining the optimum source impedance is shown in Fig. 5. The optimum source impedance can be defined as the source impedance which gives the maximum conversion efficiency at the desired harmonic. Note that the circuit in Fig. 5 is basically a comb generator. Since it is going to be used as a part of the frequency multiplier, the output circuit is not just a 50 Ω transmission line. Thus, the transmission line and the gap can be optimized to give the maximum conversion efficiency, though the output signal should be filtered further.

Once this optimum source impedance is known, an impedance matching circuit can be designed to match the diode to a 50 Ω source. Finally, the driving inductor can be realized by means of a microstrip line. Calculation of a straight microstrip line inductor is simple and an example

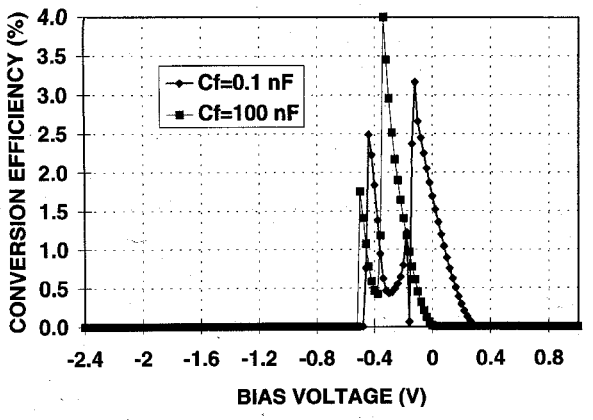

Fig. 6. Simulated resultsof conversion efficiency vs. bias voltage.

TABLE I
USED COMPUTATIONAL RESOURCES IN SIMULATIONS OF AN SRD FREQUENCY MULTIPLIER

C_f (nF)	CPU (second)	Virtual Memory Used (MB)
100	3690	3.15
0.1	1104	3.15

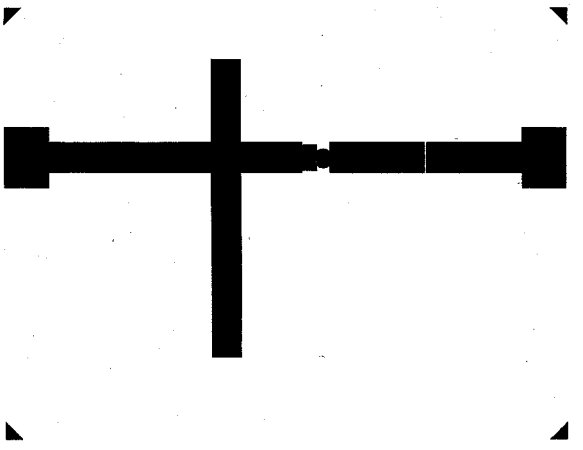

Fig. 7. Layout of an SRD comb generator. Substrate: RT/Duroid, $\varepsilon_r = 2.33$, $h = 1.57$ mm.

is given in [11]. This part of the circuit can be optimized either at this stage or together with the output circuit of the frequency multiplier at a later stage.

The design of output circuit of the frequency multiplier consists mainly of the design of a bandpass filter. The bandwidth of the filter should be determined according to the specific application. Normally, narrow band coupled line bandpass filter is used; whereas wide band bandpass filter could also be employed for a particular application [12]. The design method can be found in other literature [13], [14]. Here a microstrip coupled-line bandpass filter is designed and simulated by using MDS.

Once the designs of the comb generator and the bandpass filter are accomplished, they can be put together to form the frequency multiplier. Apparently, the filter can extract the desired harmonic from the comb generator, and drop the unwanted harmonics. However, since the output of the comb generator is very rich of harmonics and the desired harmonic could be a very high order harmonic, the effects of all those unwanted harmonics can not readily be neglected. Therefore, the input matching circuit and the output circuit consisting of a transmission line, a gap and a bandpass filter should be re-optimized to get the optimum performance, e.g., the high conversion efficiency.

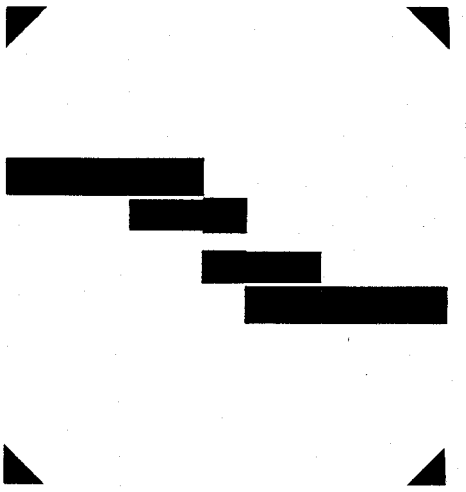

Fig. 8. Layout ofa microstrip coupled line bandpass filter. Substrate: RT/Duroid, $\varepsilon_r = 2.33$, $h = 0.79$ mm; scale: 2:1.

In order to verify the method for improving the efficiency of the CAD of the SRD frequency multiplier presented above, we designed a 10×1.25 GHz SRD microstrip frequency multiplier. A large voltage excitation source corresponding to an input power of 13 dBm at 1.25 GHz was used for the harmonic-balance simulation. At first, the circuit was optimized for a high conversion efficiency with C_f equal to 0.1 nF. Then the circuit was refined experimentally. Thereafter, the harmonic-balance analyzes with swept bias voltage were carried out with C_f equal to 0.1 nF and 100 nF and compared with the experiment.

The simulation results are shown in Fig. 6. It can be seen that the shapes of these line pairs are essentially the same. The lines with different C_f are shifted to the right or left of the other. The conversion efficiency is a little lower with lower C_f, which corresponds to the weaker nonlinearity of the model. The shifting of lines is partially due to the different degree of the nonlinearity. Furthermore, in a strongly nonlinear circuit, the low-order mixing frequencies generated by high-degree nonlinearity cannot be neglected readily; thus, the excitation of a strongly nonlinear circuit may offset the DC operating point.

The computational resources required for different C_f are listed in Table I. The results in Table I indicate that the computation time is much less for lower C_f than that for higher C_f. The comparison is made under the condition of the same memory used, as can be seen in the table. Furthermore, it should be pointed out that the simulation with higher C_f shows more trouble in convergence, especially in the case of inappropriate initial conditions.

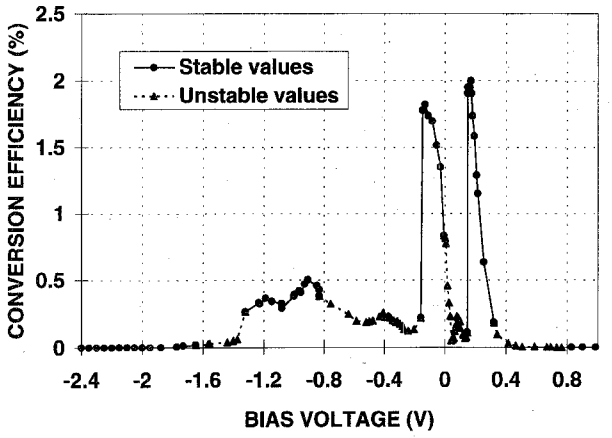

Fig. 9. Experimental results of conversion efficiency vs. bias voltage.

IV. Experiments

Experiments were done with the multiplier. The comb generator and bandpass filter were built separately. Their layouts are shown in Figs. 7 and 8, respectively. The HP ceramic packaged SRD (HP-5082-0835) was used. The substrate thickness of the comb generator was chosen to match the ceramic package. The bandpass filter could also be integrated on the same substrate as the comb generator. However, a separate bandpass filter, which has more freedom in choosing substrates, and which provides the flexibility of experimentation, was used.

The input signal was a 1.25 GHz sinusoidal signal at the power level of 13 dBm, which was measured directly at the input port of the multiplier with a spectrum analyzer (Tektronix 2782). The DC bias voltage was applied through a bias tee. The output power was measured at the 10th harmonic using the same spectrum analyzer.

The experiment was carried out by changing the bias voltage and recording output power. The conversion efficiency was calculated by dividing the output power by the available power at the input port. The measured results are shown in Fig. 9. The points connected with dashed-lines represent cases where the output signal showed spurious behavior, caused by spurious oscillations in the circuit.

Fig. 9 shows that the conversion efficiency varies with bias voltage in a similar way as in the above simulations. The lower experimental efficiency than the calculated result is caused by the loss of the circuit.

It should be noted that the parasitics arising from mounting the packaged diode have been neglected in the simulations. However, both the simulation and experiment show that the circuit is quite sensitive to the length of the transmission line between the diode and the gap in the output circuit, which is closely related to the mounting structure of the diode. Therefore, the effects of diode mounting structure should not be neglected in more accurate analyzes. Numerical electromagnetic analyzes of the effects of the diode mounting structure should be done for better modeling of the hybrid SRD frequency multiplier.

V. Conclusion

The CAD of SRD frequency multipliers can be made more efficient and easier to accomplish by the method of reducing the nonlinearity of the SRD model in the simulation. The experiment shows that the simulated results can be used to guide the SRD frequency multiplier design very well to achieve a high conversion efficiency. An efficiency of more than 2% was achieved at 12.5 GHz with a 10th harmonic multiplier using microstrip circuits. In general, the method could also be applied to CAD of circuits using other very strong nonlinear devices.

Acknowledgment

The authors would like to express their special thanks to M. Hytönen for her help in manufacturing the circuit boards.

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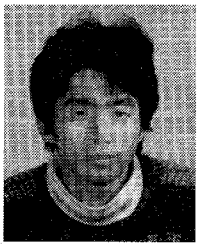

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